WHAT IS CLAIMED IS:

1. A method for use in a system for testing a semiconductor wafer, said system comprising a stage for moving said wafer into and out of contact with a plurality of probes, said method comprising:

monitoring a voltage on a power source to one of said probes; and

if said voltage exceeds a predetermined threshold during a move of said stage, signaling an arc condition.

2. The method of claim 1, wherein said monitoring comprises comparing said voltage on said power source to a reference voltage.

3. The method of claim 2, wherein said signaling an arc condition comprises enabling an output of a result of said comparing during said move of said stage.

4. The method of claim 3, wherein said enabling comprises:

receiving an indication that a move of said stage is to take place; and

enabling said output of said result in response to said indication that a move of said stage is to take place.

5. The method of claim 4, wherein said enabling further comprises:

receiving an indication that said move has been completed; and

disabling said output of said result in response to said indication that said move has been completed.

6. The method of claim 1, wherein said signaling an arc condition comprises activating an indicator.

7. The method of claim 1, wherein said signaling an arc condition comprises lighting a light.

8. The method of claim 1, wherein said signaling an arc condition comprises sending a message.

9. The method of claim 1 further comprising:

monitoring voltages on a plurality of power sources to a plurality of said probes; and

if at least one of said voltages exceeds a predetermined threshold during said move of said stage, signaling an arc condition.

10. An apparatus comprising:

a comparator having an input connected to a reference voltage and another input connected to a power source to a test probe for contacting a semiconductor wafer;

a latch having an input connected to an output of said comparator;

enabling means for enabling said latch only in connection with a move of said wafer with respect to said probe; and

signaling means for signaling an arc condition if said output of said latch indicates that said output of said comparator was triggered while said latch is enabled.

11. The apparatus of claim 10, wherein said reference voltage corresponds to a voltage level sufficient to cause an arc between said probe and said wafer.

12. The apparatus of claim 10, wherein said enabling means enables said latch prior to said move of said wafer and disables said latch after completion of said move.

13. The apparatus of claim 10, wherein said signaling means activates an indicator.

14. The apparatus of claim 10, wherein said signaling means lights a light.

15. The apparatus of claim 10, wherein said signaling means sends a message.

16. The apparatus of claim 10 further comprising:

a plurality of said comparators, each having an input connected to said reference voltage and another input connected to a power source to one of a plurality of said test probes; and

a plurality of said latches, each having an input connected to an output of one of said comparators.

17. The apparatus of claim 10, wherein said another of said inputs of said comparator is indirectly connected to said power source to said test probe.

18. The apparatus of claim 17, wherein said another of said inputs of said comparator is capacitively connected to said power source to said test probe.

19. The apparatus of claim 10, wherein

said test probe is disposed on a probe card assembly, and

said comparator and said latch are disposed on a substrate that is pluggable into a socket on said probe card assembly.

20. An apparatus for testing a semiconductor wafer, said apparatus comprising:

moving means for moving said wafer into and out of contact with probes of a probe card assembly;

monitoring means for monitoring a voltage level of power supplied to one of said probes;

signaling means for signaling an arc condition if said voltage exceeds a predetermined threshold during a move of said wafer.

21. The method of claim 20, wherein:

said monitoring means further monitors voltage levels of power supplied to a plurality of said probes; and

said signaling means further signals an arc condition if said voltage of power supplied to at least one of said probes exceeds said predetermined threshold.